

FIG. 1

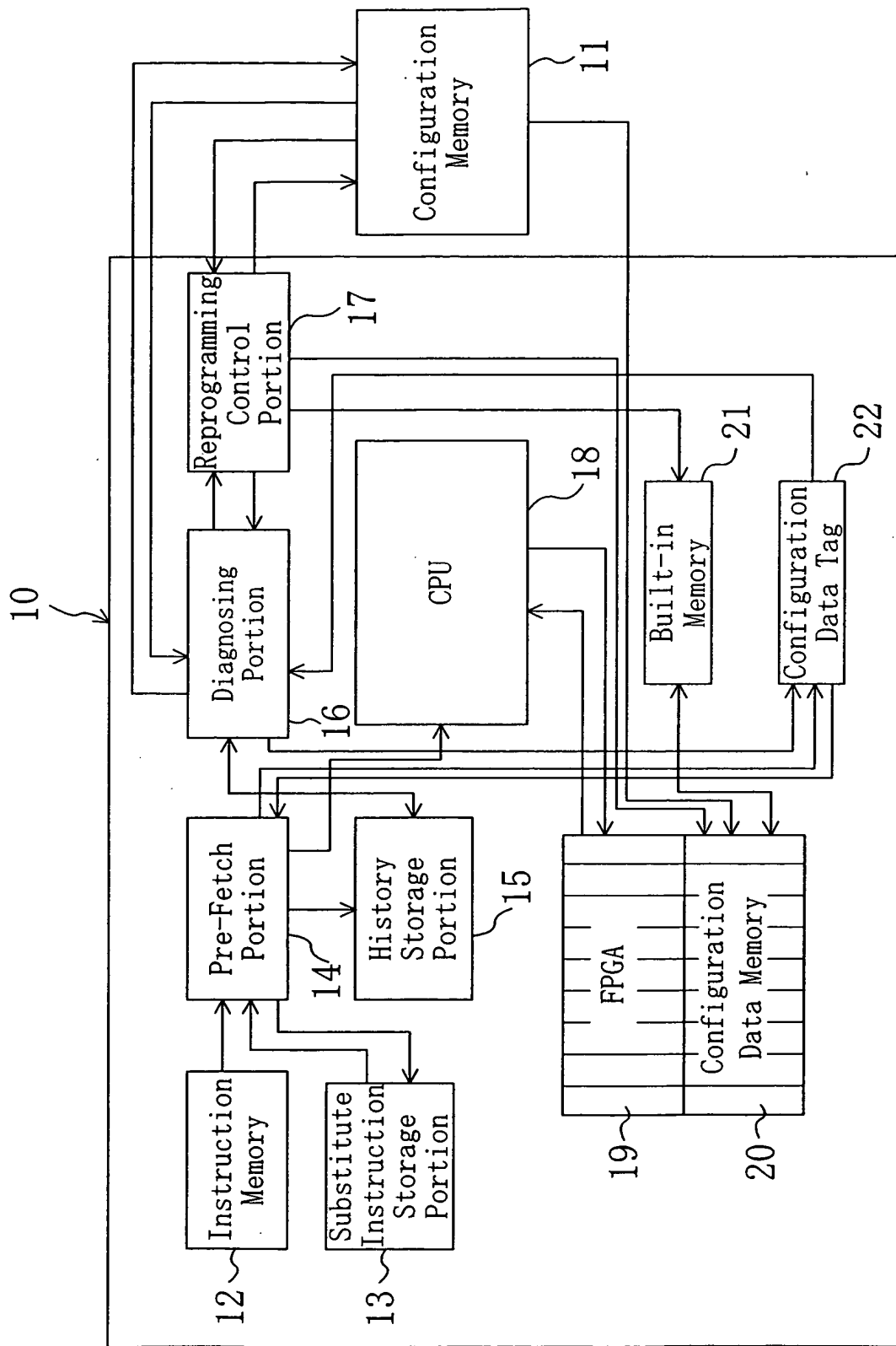


FIG. 2

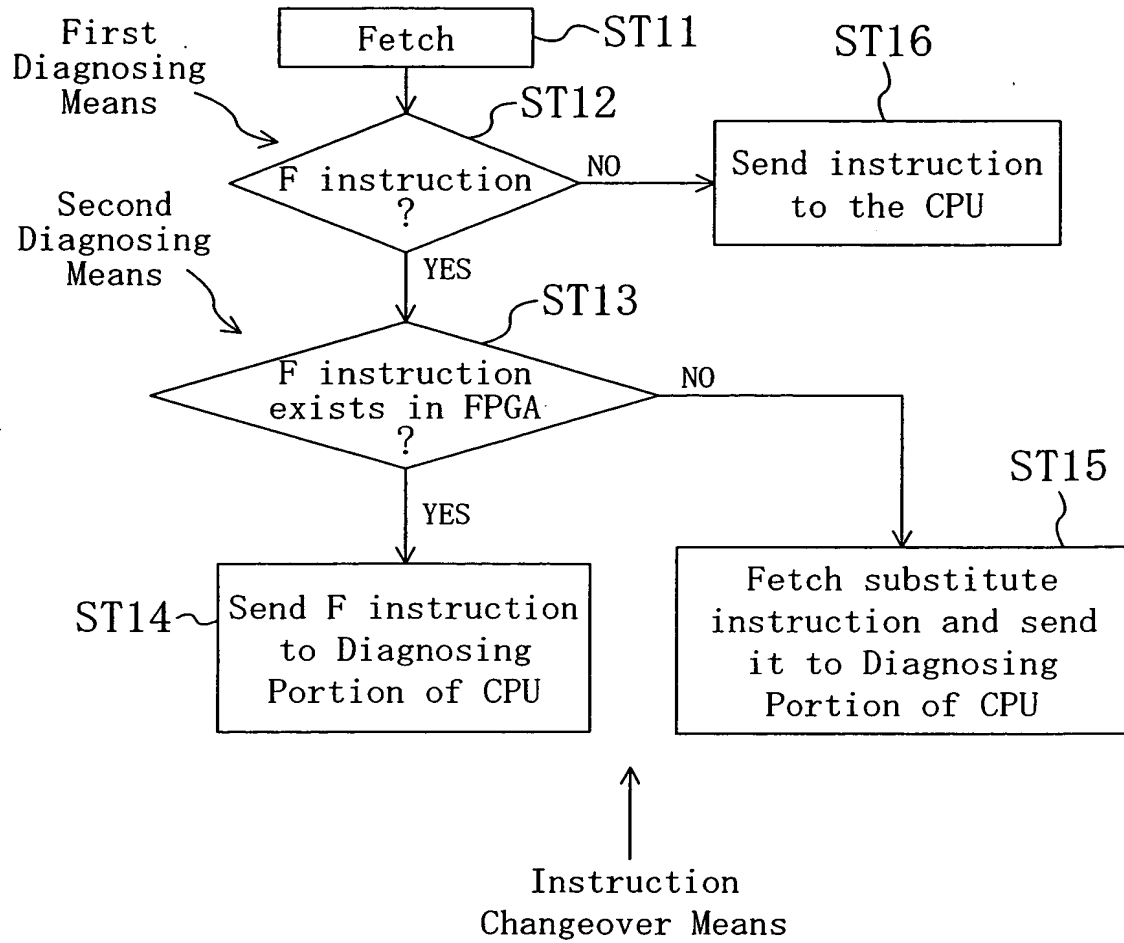


FIG. 3

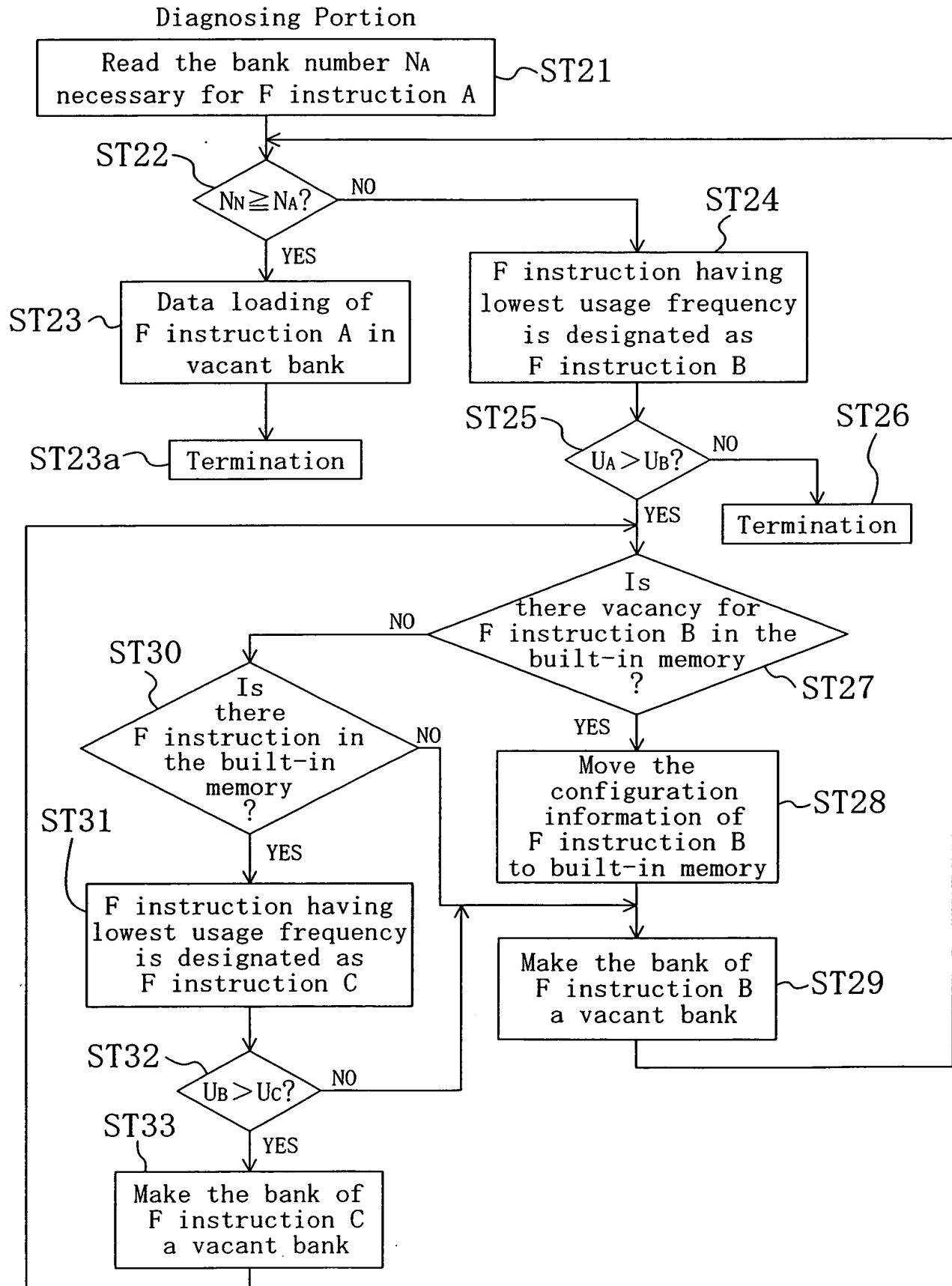


FIG. 4

Instructions		Comment
ADD	D1, D2	#D1+D2→D2
LSR	D3, D2	#D2 (D3)bit shift-right→D2

FIG. 5

Bank0 ID=1	Bank1 ID=1	Bank2 ID=4	Bank3 ID=4	Bank4 ID=4	Bank5 ID=0	Bank6 ID=0	Bank7 ID=0
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FIG. 6A

FPGA 1 D1, D2, D3 #D1+D2 (D3)bit shift-right→D2

FIG. 6B

ADD D1, D2 #D1+D2→D2

LSR D3, D2 #D2 (D3)bit shift-right→D2

FPGAend # Termination of substitute instruction

FIG. 7

Both F instruction and substitute instruction are described.

FPGA 0 D1, D2, D3(addr) #D1+D2 (D3)bit shift-right→D2

#In case F instruction is
executed, skip to (addr)

ADD D1, D2 #D1+D2→D2 Substitute instruction
from here

LSR D3, D2 #D2 (D3)bit shift-right→D2 Substitute
instruction up to
this point

(Next instruction) # This is the address shown
by (addr)

FIG. 8

ADD D1, D2 #D1+D2→D2
LSR D3, D2 #D2 (D3)bit shift-right→D2

FIG. 9

ID	Instruc- tions	Corresponding Configuration Data	Number of Banks
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FIG. 10

1	ADD D1, D2 LSR D3, D2	Corresponding Configuration Data	1
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FIG. 11

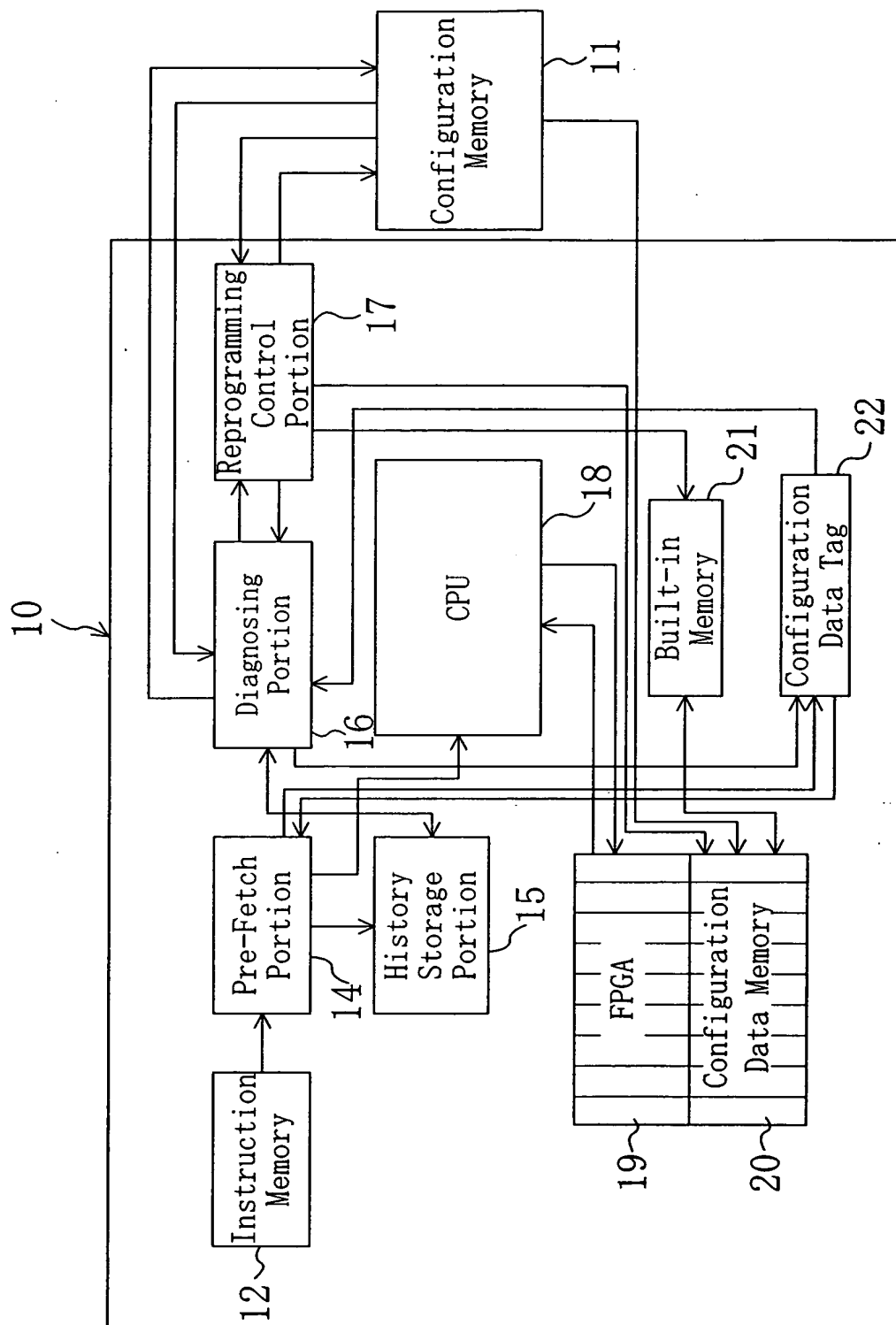


FIG. 12

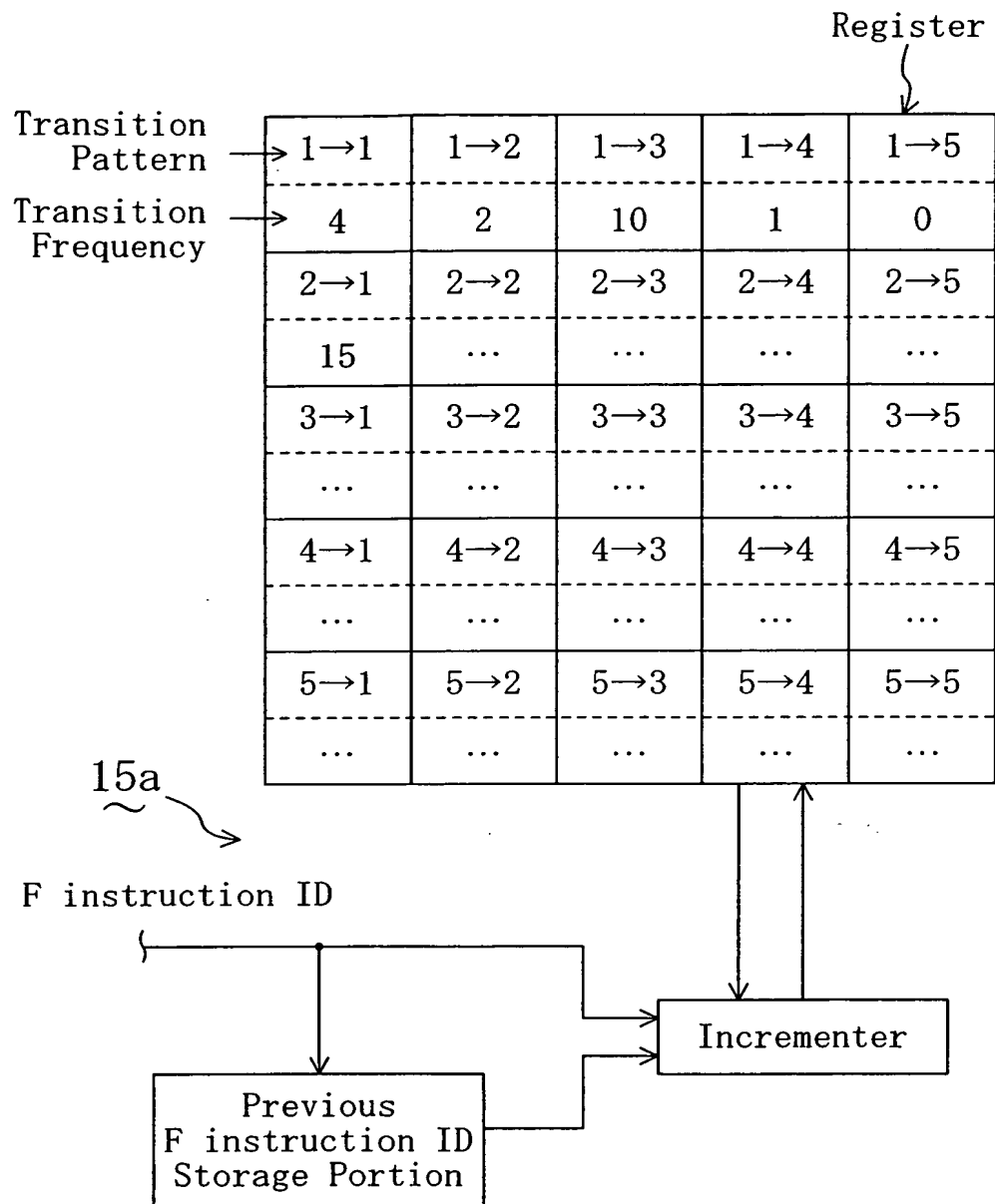


FIG. 13

